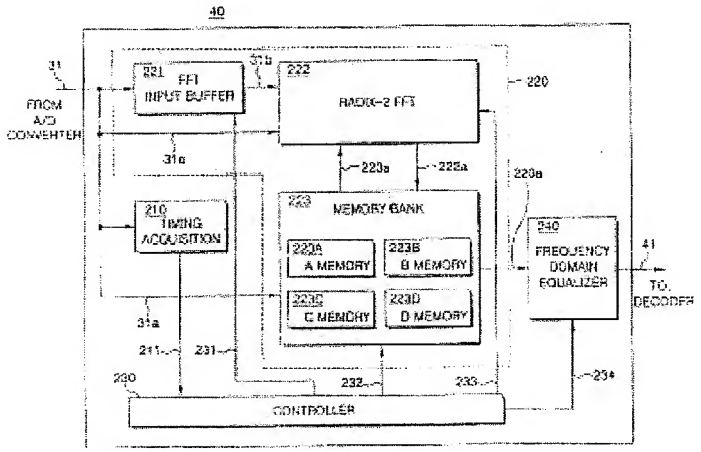
REMARKS

Applicants appreciate the continued thorough examination of the present application that is reflected in the Office Action of August 22, 2007. Claims 1-19 are pending in the application. Applicants particularly appreciate the indication that Claims 8-11 are allowed. While Claim 12 was indicated as rejected on the Office Action Summary, the body of the Office Action does not provide any basis for rejection of Claim 12. Moreover, as Claim 12 is dependent from allowable Claim 8, the Applicants assume that the Office Action should have indicated that Claim 12 is allowable. If this understanding is incorrect, the Applicants respectfully request clarification. In the following remarks, Applicants will demonstrate that the remaining claims are patentable over the cited references.

Claims 1-7 Are Patentable Over the Cited References

In the Office Action, Claim 1 was rejected under 35 USC § 103(a) as unpatentable over U.S. Patent No, 5,778,073 to Busching et al. ("Busching") in view of U.S. Patent No. 5,732,113 to Schmidl et al. ("Schmidl"). Office Action, page 3. Applicants respectfully submit that the cited references do not, alone or in combination, teach or suggest the recitations of Claim 1 for at least the reasons explained below. Accordingly, Applicants respectfully request that the rejection of Claim 1 be withdrawn.

Embodiments of the invention are directed to Fast Fourier Transform (FFT) processors for demodulating an orthogonal frequency division multiplexing (OFDM) signal. Figure 3 of the present application is reproduced below for the Examiner's convenience.



In particular, Claim 1 recites an FFT processor for demodulating an OFDM signal having a symbol, the symbol including a first long preamble and first data. The FFT processor of Claim 1 includes:

> ...
> a timing acquisition section that is configured to output a timing signal in response to detecting an end point of the first long preamble;
> a controller that is configured to output a first control signal and a second control signal in response to the timing signal;
> a signal converter that is configured to store the first long preamble in response to the first control signal, to transform the first long preamble by a fast Fourier transform into a second long preamble, to store the second long preamble, to transform sequentially the first data by the fast Fourier transform into second data as the first data sequentially is received, to output the second long preamble, to store the second data, and to output the second data; and
> a frequency domain equalizer that is configured to synchronize the second long preamble and the second data that is output from the signal converter in response to the second control signal with a clock frequency of the fast Fourier transform processor, and to output the synchronized second long preamble and second data.

As explained in the application, an OFDM symbol includes a preamble and data. See Specification, Fig. 1. Portions of the preamble are inspected by an OFDM receiver to determine carrier frequency offset and for synchronization. Specification, para. [0007]. As further explained in the Specification, embodiments of the invention can reduce the total FFT processing time by processing the preamble and the data according to systems/methods described therein.

In particular, Claim 1 recites:

> a signal converter that is configured to store the first long preamble in response to the first control signal, to transform the first long preamble by a fast Fourier transform into a second long preamble, to store the second long preamble, to transform sequentially the first data by the fast Fourier transform into second data as the first data sequentially is received, to output the second long preamble, to store the second data, and to output the second data;

Thus, according to Claim 1, the signal converter is configured to transform the first long preamble by FFT into a second long preamble, to store the second (i.e., transformed) long preamble, and to output the second long preamble.

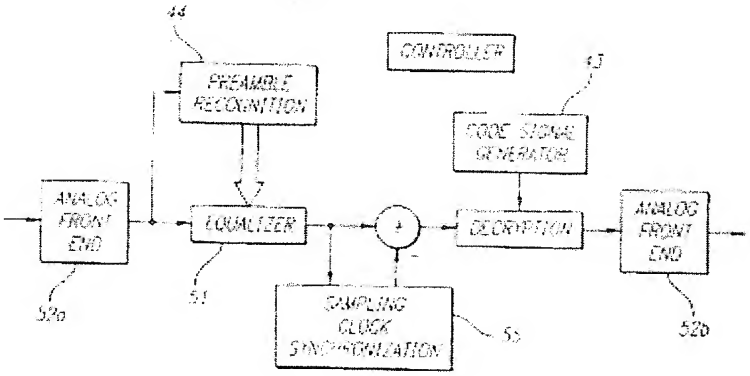
Claim 1 further recites:

a frequency domain equalizer that is configured to synchronize the second long preamble and the second data that is output from the signal converter in response to the second control signal with a clock frequency of the fast Fourier transform processor, and to output the synchronized second long preamble and second data.

In rejecting Claim 1, the Office Action asserts that Busching discloses a receiver apparatus including a timing acquisition section, a controller and a frequency domain equalizer as recited in Claim 1. Office Action, page 3. The Office Action further asserts that Busching discloses an FFT whose operation is controlled by a control signal based on the detection of a preamble in an input signal. Id.

Initially, Applicant notes that Busching is not directed to an OFDM receiver, see Busching Abstract, and accordingly does not perform FFT processing of an OFDM signal as recited in Claim 1. Furthermore, Busching does not teach or suggest a frequency domain equalizer as recited in Claim 1. While Busching Figure 5 shows an equalizer 51, the equalizer 51 of Busching operates on an sampled time domain signal output by the analog front end 52a. Busching Fig. 5 is reproduced below for convenience.

FIG. 5



As the received signal is not an OFDM signal, no FFT processing is performed during the demodulation thereof. As explained in Busching: "The received signal is converted by the analog front end 52 into a digital signal with, for example, an 8 kHz sampling frequency and a 16 bit word length. This signal passes through the equalizer 51, whose object is equalization of the transmission channel as explained below." Busching, col. 11, lines 50-54. There is no indication in Busching that the equalizer is a frequency domain equalizer, which

is to be expected since Busching does not disclose an OFDM receiver, so there is no FFT-processed frequency domain signal to equalize.

Furthermore, although Busching discloses FFT processing of a signal preamble for generating filter coefficients for the equalizer 51, there is no indication that the output of the FFT processing of Busching is a transformed preamble that is either (i) stored, (ii) output, or (iii) synchronized with a clock frequency of the FFT processor.

The Office Action concedes that "Busching does not expressly disclose that the equalizer synchronizes the output of the signal converter in with a clock frequency of the fast Fourier transform processor, and output s a synchronized second long preamble and second data." Office Action, pages 3-4. Nevertheless, the Office Action asserts that "it would have been obvious to one of ordinary skill in the art at the time of the invention to synchronize the output of the signal converter with a clock frequency of the FFT to synchronously process the data and preamble and therefore prevent having overflows of data." Office Action, page 4. However, this assertion overlooks the fact that the data signal of Busching is **not** processed with an FFT processor. Rather, the FFT processor of Busching is only used to find filter coefficients using the preamble. Thus, contrary to the assertion in the Office Action, a skilled person would not modify Busching to synchronize the output of the FFT processor with a clock frequency of the FFT to synchronously process the data and the preamble of the signal.

The Office Action further concedes that Busching does not teach "that the signal converter is configured to store the first long preamble in response to the first control signal, transform the first long preamble by a fast Fourier transform into a second long preamble, store the second long preamble, transform sequentially the first data by the fast Fourier transform into second data as the first data sequentially is received, output the second long preamble, store the second data, and to output the second data." In an effort to supply the numerous missing recitations, the Office Action cites Schmidl and states that it would have been obvious to modify Busching as suggested by Schmidl. Office Action, pages 4-5. However, the attempt to combine Schmidl with Busching fails, because Busching cannot properly be combined with Schmidl in the manner described in the Office Action.

The Office Action states at the bottom of page 4 that "it would have been obvious to modify Busching as suggested by Schmidl to provide fast timing acquisition of the received signal and also enable synchronization to the burst signal for proper reception of the burst data frame." Schmidl is directed to methods of performing rapid timing synchronization,

carrier frequency synchronization, and sampling rate synchronization of a receiver to an OFDM signal. See Schmidl, Abstract. As such, a skilled person would not modify a non-OFDM system such as Busching to use the synchronization techniques of Schmidl. In particular, Schmidl teaches methods that employ a particular arrangement of training sequences in an OFDM symbol stream to perform timing, carrier frequency, and sampling rate synchronization. See Schmidl, Fig. 6 and accompanying text. A skilled person simply could not use such techniques in a non-OFDM system, and therefore would not modify Busching as asserted in the Office Action. Accordingly, Claim 1 is patentable over the cited references.

Claims 2-4, 6 and 7 were rejected under 35 USC § 103(a) as unpatentable over Busching and Schmidl in view of U.S. Publication No. 2003/0050945 to Chen et al. ("Chen"). Office Action, page 5. Claim 5 was rejected under 35 USC § 103(a) as unpatentable over Busching, Schmidl and Chen and further in view of U.S. Patent No. 6,098,088 to He et al. ("He"). Dependent Claims 2-7 are patentable at least per the patentability of Claim 1. Moreover, many of these claims are separately patentable over the cited references. For example, Claim 2 recites (emphasis added):

> an input buffer that is configured to temporarily store the first data in response to the first control signal, and to output the temporarily stored first data;
>
> a memory bank that is configured to store the first long preamble and the first data, to store the second long preamble and the second data, and to output the stored first and second long preamble and the stored first and second data in response to the first control signal; and
>
> a frequency converter that is configured to read the first long preamble stored in the memory bank in response to the first control signal, to transform the first long preamble into a second long preamble in a frequency domain, to store the second long preamble in the memory bank, to transform the first data provided from the input buffer and the first data directly input to the frequency converter into second data in the frequency domain in response to the first control signal, and to store the second data in the memory bank.

As explained in the specification, while the preamble is being processed by the frequency converter (FFT unit 222), N/2 samples of the input symbol are stored in the input buffer. See Specification, page 8, lines 24-27. After the preamble has been processed, the N/2 samples of the input signal from the input buffer are provided to the FFT unit 222, and N/2 samples are directly input into the FFT unit 222. See Specification, page 10, lines 9-11.

The FFT unit 222 then transforms the data provided by the input buffer and the data that is input directly into the frequency converter into second (i.e. transformed) data. Id.

The Office Action does not indicate how the cited references teach or suggest a frequency converter that is configured to transform the first data provided from the input buffer and the first data directly input to the frequency converter into second data in the frequency domain. Moreover, Applicants can find no teaching of such a structure in the cited references. Applicants therefore submit that Claim 2 is patentable over the cited references for at least these additional reasons.

Claims 13-17 Are Patentable Over the Cited References

Claim 13 was rejected under 35 USC § 103(a) as unpatentable over U.S. Patent No. 5,550,812 to Philips, Applicant's Background and Busching in view of Schmidl. Claims 14-17 were rejected under 35 USC § 103(a) as unpatentable over Philips, Applicant's Background, Busching and Schmidl in view of Chen.

Claim 13 recites an FFT processor that includes:

> a timing acquisition section that is configured to output a timing signal in response to detecting an end point of the first long preamble;
>
> a controller that is configured to output a first control signal and a second control signal in response to the timing signal;
>
> a signal converter that is configured to store the first long preamble in response to the first control signal, to transform the first long preamble by a fast Fourier transform into a second long preamble, to store the second long preamble, to transform sequentially the first data by the fast Fourier transform into second data as the first data sequentially is received, to output the second long preamble, to store the second data, and to output the second data; and
>
> a frequency domain equalizer that is configured to synchronize the second long preamble and the second data that is output from the signal converter in response to the second control signal with a clock frequency of the fast Fourier transform processor, and to output the synchronized second long preamble and second data.

The Office Action concedes that these recitations are not taught by Philips or Applicant's Background section, but contends that these recitations are taught by a combination of Busching and Schindl. Office Action, pages 8-10. However, as explained above with respect to Claim 1, the combination of Busching and Schindl is improper, and in any case does not teach or suggest each and every one of the above-quoted recitations. Accordingly, Claim 13 is patentable for at least similar reasons as Claim 1. Claims 14-17 are

patentable at least per the patentability of Claim 13. Moreover, Claim 14 is separately patentable for at least similar reasons as explained with respect to Claim 2.

Claims 18 and 19 Are Patentable Over the Cited References

Claims 18 and 19 were rejected under 35 USC § 103(a) as unpatentable over Schmidl in view of Chen.

Claim 18 recites as follows:

> 18. A Fast Fourier Transform (FFT) processor for processing an Orthogonal Frequency Division Multiplexing (OFDM) signal having a symbol, the symbol including a first long preamble and first data, the FFT processor comprising:
> an input buffer that is configured to temporarily store the first data;
> a memory bank that is configured to store the first long preamble; and
> an FFT unit that is configured to transform the first long preamble in the memory bank into a second long preamble in a frequency domain and to store the second long preamble back into the memory bank, to transform the first data that is temporarily stored in the input buffer into second data in the frequency domain and to store the second data into the memory bank.

The Office Action contends that Schmidl Figure 5 shows an input buffer 122, a memory 122, and an FFT unit 126 that is configured to transform first data that is stored in the input buffer 122 into second data in the frequency domain and to store the second data into the memory 122. Office Action, page 13. However, the Office Action does not cite to specific passages of Schmidl that show this operation, nor can Applicants find any such teaching in Schmidl. Rather, as shown in Schmidl Figures 3 and 5, transformed data output by the FFT unit 126 is output not to the memory 122 but to a decoder 102. As explained in Schmidl, the FFT 126 performs the functions of the DSP 100 of Figure 3, See Schmidl, col. 11, lines 46-48: "Synchronization apparatus 120 is essentially a DSP system that takes the place of the prior art DSP 100 in OFDM receiver 60 of FIG. 3." Schmidl further explains that the DSP 100 delivers the demodulated sub-symbols from each OFDM symbol to a decoder 102, which recovers the originally transmitted information. Schmidl, col. 4, lines 39-47. Thus, Schmidl does not teach or suggest an FFT unit that is configured to transform the first data that is temporarily stored in the input buffer into second data in the frequency domain and to store the second data into the memory bank, as recited in Claim 18.

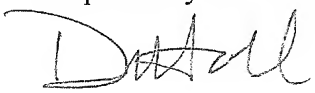
Chen does not supply the missing recitations, as Chen is cited merely to show the possible existence of a memory bank. Office Action, page 13. Accordingly, Applicants respectfully submit that Claim 18 is patentable over the cited references. Claim 19 is patentable at least per the patentability of Claim 18.

CONCLUSION

In view of the foregoing discussion, Applicants respectfully submit that the application is in condition for allowance, and request issuance of a Notice of Allowance in due course.

If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,



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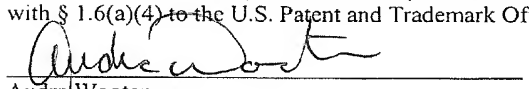

Audra Wooten
Date of Signature: November 14, 2007